AMENDMENTS TO THE SPECIFICATION

The amended abstract of the disclosure was objected to because it was not provided on a separate sheet. The amended abstract has been submitted on a separate sheet to overcome this objection.

CLAIM OBJECTIONS

Claims 5 and 14 are objected to for minor informalities and have been amended in accordance with the Examiner's suggestions to correct the informalities.

35 U.S.C. §112 CLAIM REJECTIONS

Claims 5-8 and 14-17 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite. Claims 2, 3, 4, 11, 12, and 13 have been amended to overcome the rejection under 35 U.S.C. §112.

REMARKS

Claims 1-8 and 10-17 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,470,429 to Jones (hereinafter "Jones") in view of U.S. Patent No. 6,134,641 to Anand (hereinafter "Anand").

In the rejection of independent claims 1 and 10, Examiner correctly states that "Jones does not teach the bridge performing an uncacheable remote access to the cacheable coherent memory space of the first data processing system." Examiner seeks to use Anand to supply a teaching of "using [an] uncacheable request to access a cacheable coherent memory space," (emphasis added) citing column 5, lines 40-45 and column 9, lines 9-12. Applicants respectfully submit that Amand does not teach the use of an uncacheable request to access a cacheable coherent memory space.

It is well known in the art that a cacheable memory space can be either coherent or noncoherent. Applicants' independent claims 1 and 10 recite that a bridge in a second data processing system is "operable to perform an uncacheable remote access to said cacheable coherent memory space" of a first data processing system. This feature is not taught by Anand.

Anand teaches a four-step process for mapping non-cacheable memory addresses to cacheable memory addresses:

> The first stage 210 comprises the step of setting up a virtual peripheral device in the computer system. The second stage 220 comprises the step of allocating a region in the computer system's non-cacheable address space to the virtual peripheral device. The third stage 230 comprises the step of allocating a region in the computer system's cacheable address space for the virtual peripheral device. Lastly, the fourth stage 240 comprises the step of mapping the range of non-cacheable address space to the range of cacheable address space such that accesses to the range of non-cacheable address space are automatically forwarded to corresponding addresses in the cacheable address space. [Column 5, lines 34-45 (emphasis added)]

The non-cacheable address block is implemented by "tricking" the operating system at boot-up.

> In step 320, upon reading the special configuration registers, configuration software will treat the special configuration registers as if they are identifying an actual peripheral device. Consequently, computer system 100 will be tricked to set aside system resources for virtual peripheral device 165 according to the contents of the special configuration registers. Significantly, the special configuration registers include a base address within a non-cacheable peripheral I/O address space such that the I/O addresses assigned to virtual peripheral device 165 will be non-cacheable. [Column 7, lines 21-29

The portions of the Anand reference cited by Examiner do not specify whether the cacheable memory space is coherent or noncoherent. As discussed above, the Anand reference fails to supply the limitation recited in independent claims 1 and 10 of a bridge in a second data processing system is "operable to perform an uncacheable remote access to said cacheable coherent memory space" of a first data processing system. Therefore, the combination of Jones and Anand fails to teach meet the requirements of "an uncacheable request to access a cacheable coherent memory space.

Applicant respectfully submits that Examiner has failed to meet the requirements of 35 U.S.C. §103(a) in applying the combination of Jones and Anand as a basis for rejecting independent claims 1 and 10 and, therefore, the rejection of these claims should be removed. Furthermore, dependent claims 2-8 and 11-16 are allowable as being dependent on an allowable base claim.

In view of the remarks set forth herein, Applicants respectfully submit that all pending claims are in condition for allowance. Accordingly, Applicants request that the rejection of

claims 1-8 and 10-16 be withdrawn and that a Notice of Allowance be issued. Nonetheless, should any issues remain that might be subject to resolution through a telephone interview, the Examiner is requested to telephone the undersigned at 512-338-9100.

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Respectfully submitted,

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